

FIG. 1
(Prior Art)

The diagram illustrates a radio receiver system 200. An antenna 102 is connected to a Front-End Processor 104. The Front-End Processor 104 is connected to a Decimation-Interpolation Circuit 202, which is in turn connected to a Base Band Processor 204. The Base Band Processor 204 has an output line. A Micro-Processor/Controller 108 is connected to a bus 110, which is also connected to the Front-End Processor 104, the Decimation-Interpolation Circuit 202, and the Base Band Processor 204.

FIG. 2

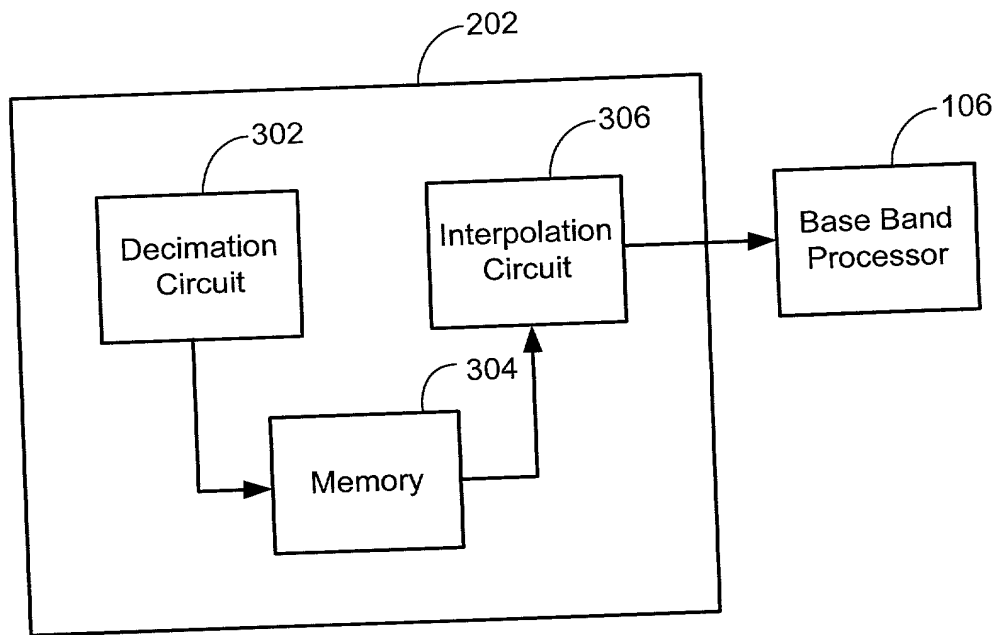


FIG. 3